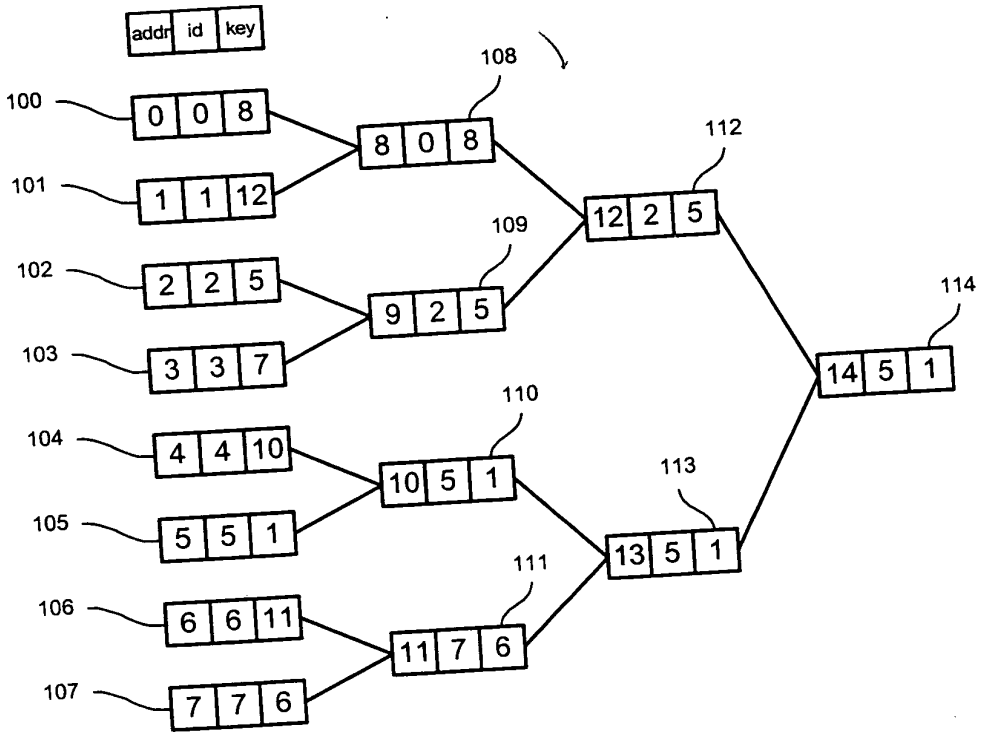

Figure 1

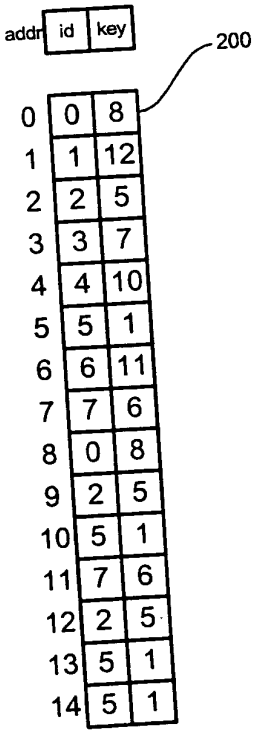

Figure 2

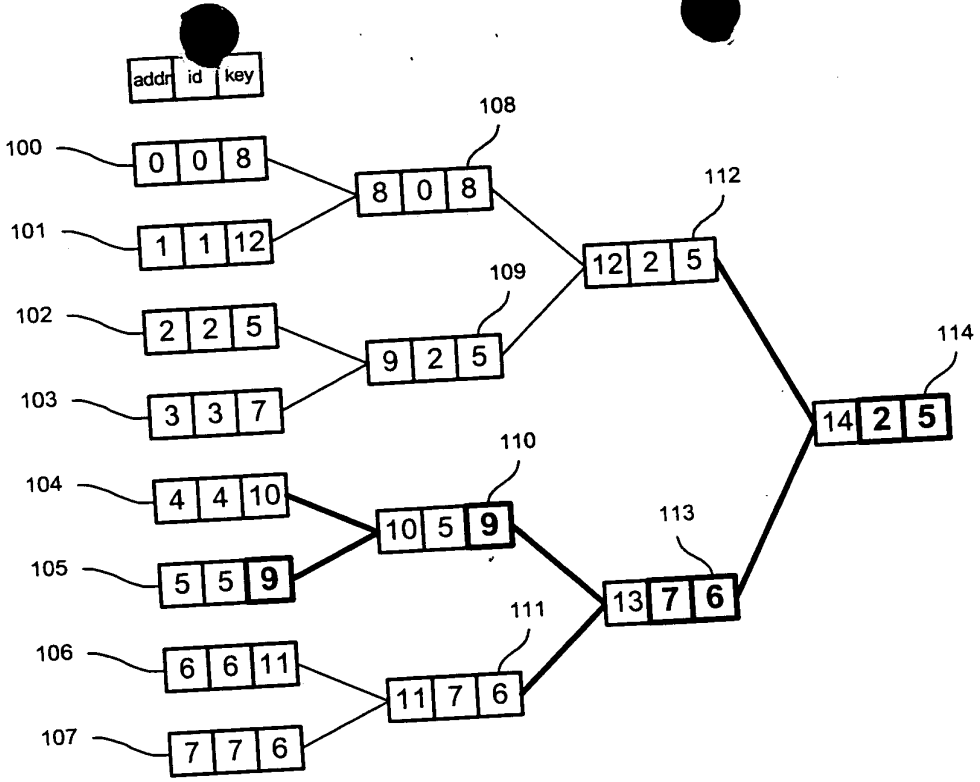

Figure 3

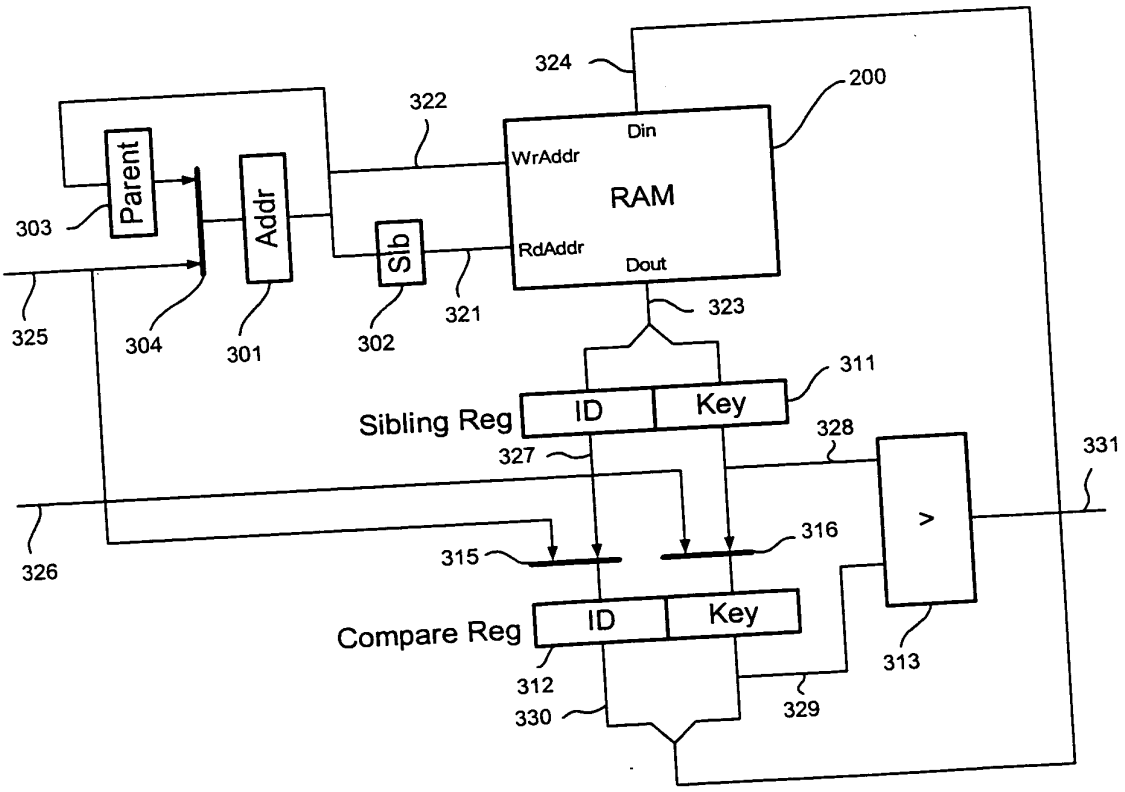

Figure 4

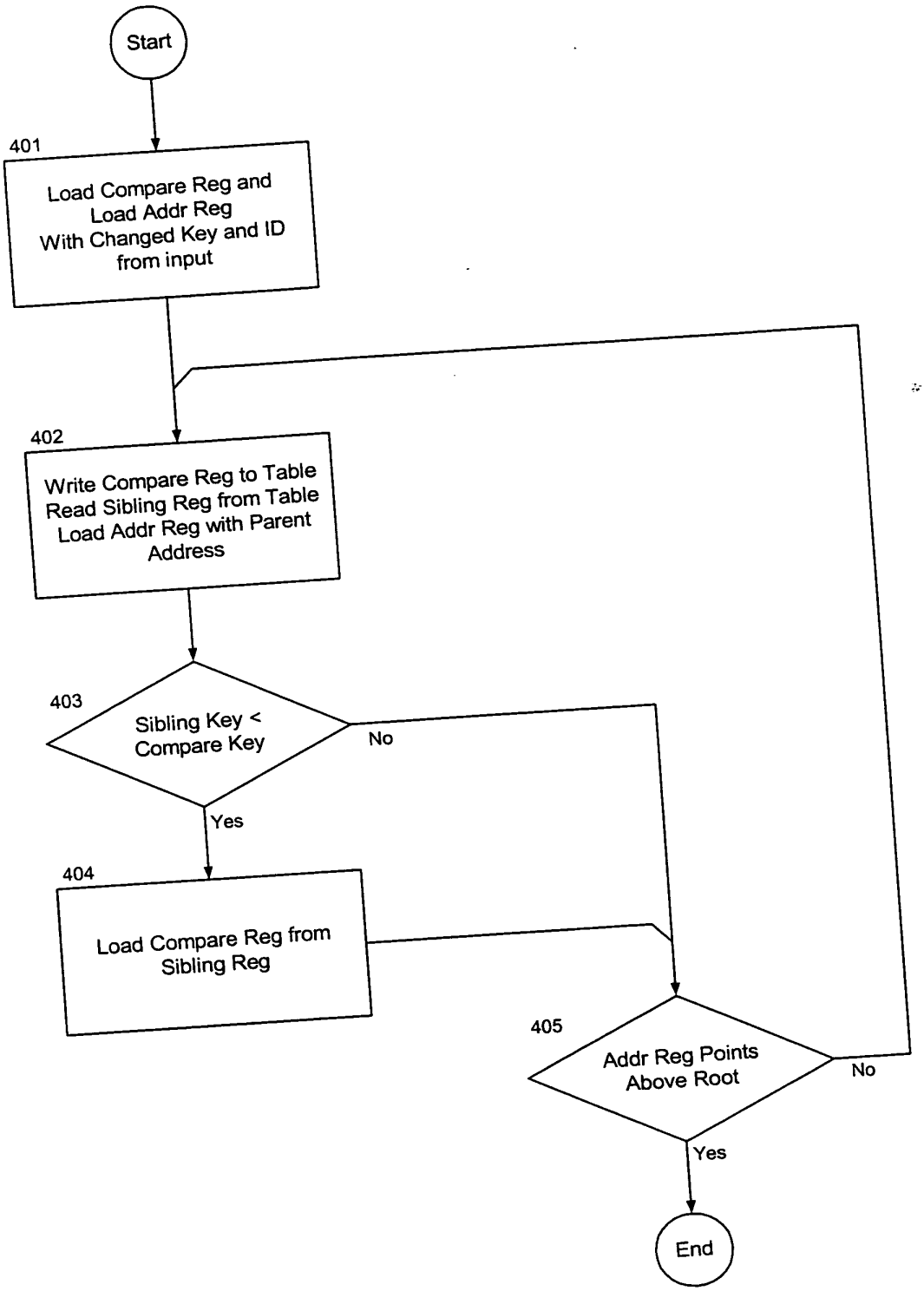
Start
401
Load Compare Reg and
Load Addr Reg
With Changed Key and ID
from input
402
Write Compare Reg to Table
Read Sibling Reg from Table
Load Addr Reg with Parent
Address
403
Sibling Key <
Compare Key
No
Yes
404
Load Compare Reg from
Sibling Reg
405
Addr Reg Points
Above Root
No
Yes
End

Figure 5

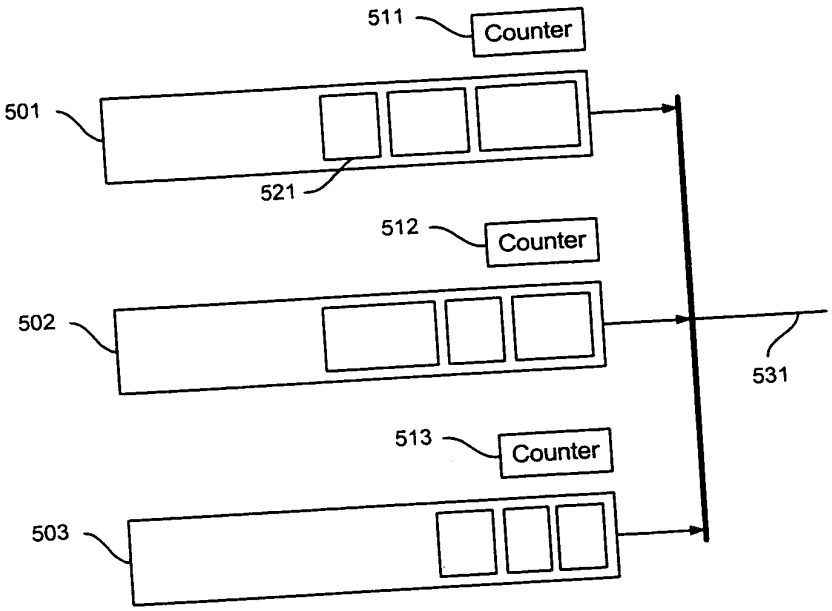

Figure 6
Prior Art

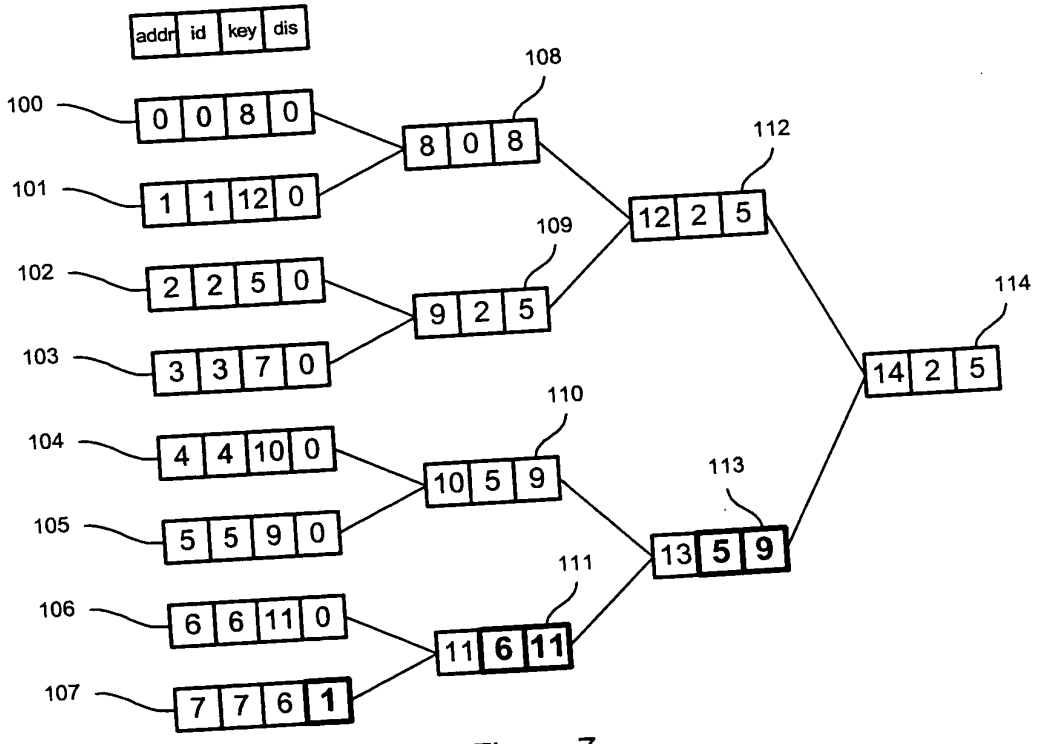

Figure 7

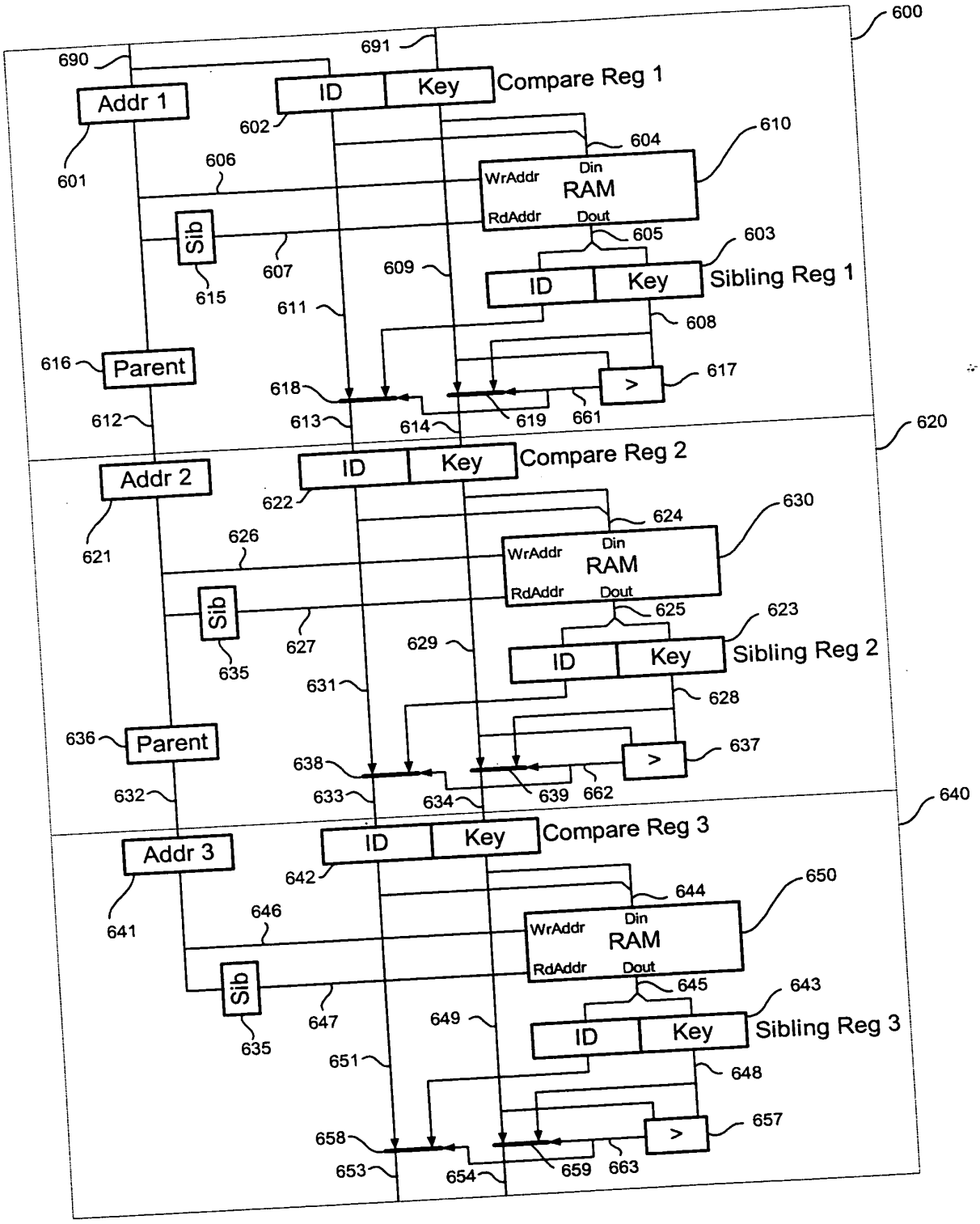
600
690
691
Addr 1
ID
Key
Compare Reg 1
602
604
610
601
606
WrAddr
Din
RAM
RdAddr
Dout
Sib
605
603
607
609
ID
Key
Sibling Reg 1
615
611
608
616
Parent
618
617
>
612
613
614
619
661
620
Addr 2
ID
Key
Compare Reg 2
622
624
630
621
626
WrAddr
Din
RAM
RdAddr
Dout
Sib
625
623
627
629
ID
Key
Sibling Reg 2
635
631
628
636
Parent
638
637
>
632
633
634
639
662
640
Addr 3
ID
Key
Compare Reg 3
642
644
650
641
646
WrAddr
Din
RAM
RdAddr
Dout
Sib
645
643
647
649
ID
Key
Sibling Reg 3
635
651
648
658
657
>
653
654
659
663

Figure 8

Register	Cycle				
	1	2	3	4	5
Addr 1	5	7	2		
Comp 1	5.9	7.d	2.15		
Sib 1	4.10	6.11	3.7		
Addr 2		10	11	9	
Comp 2		5.9	6.11	3.7	
Sib 2		7.6	5.9	0.8	
Addr 3			13	13	12
Comp 3			7.6	5.9	3.7
Sib 3			2.5	2.5	5.9
Result			2.5	2.5	3.7

Figure 9

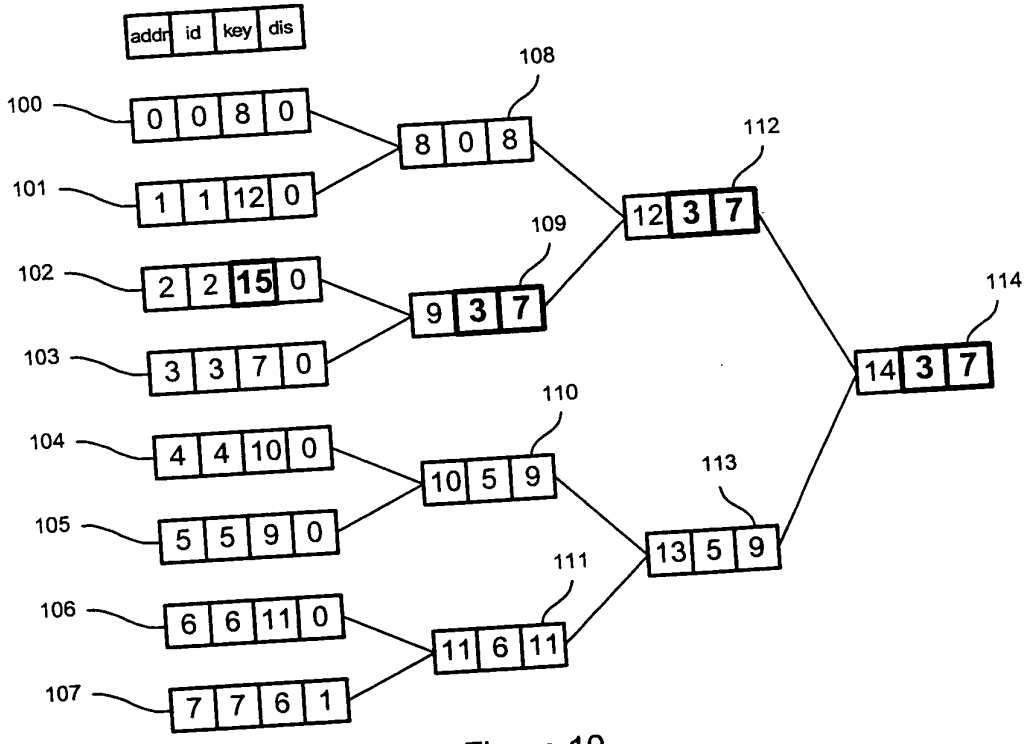

Figure 10

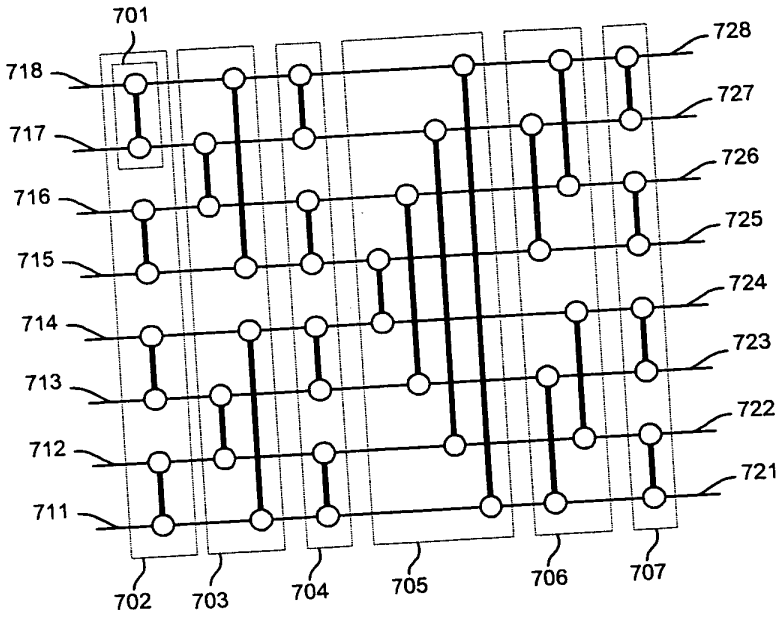

Figure 11

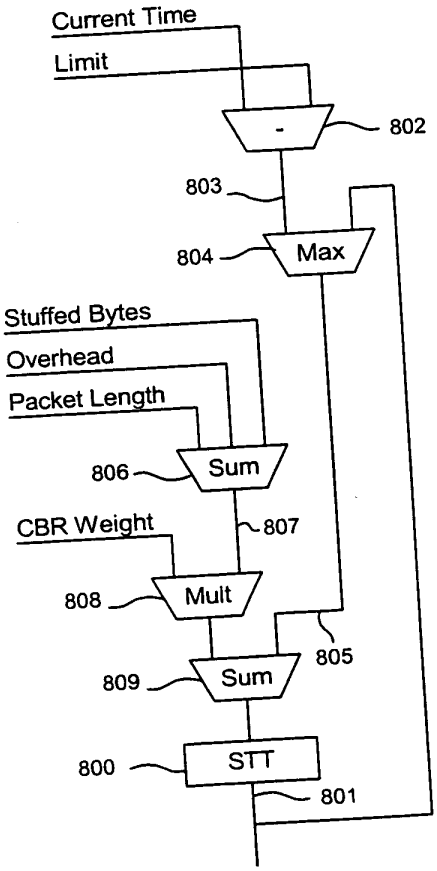

Figure 12

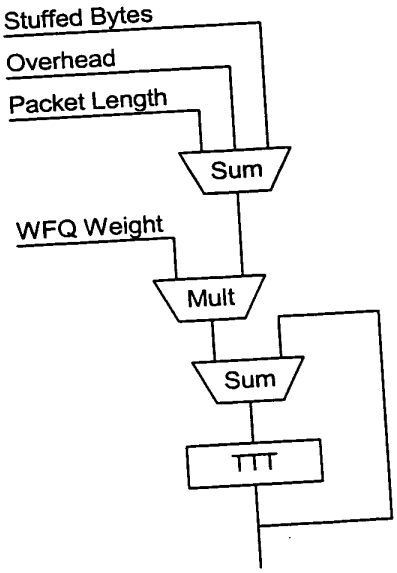

Figure 13

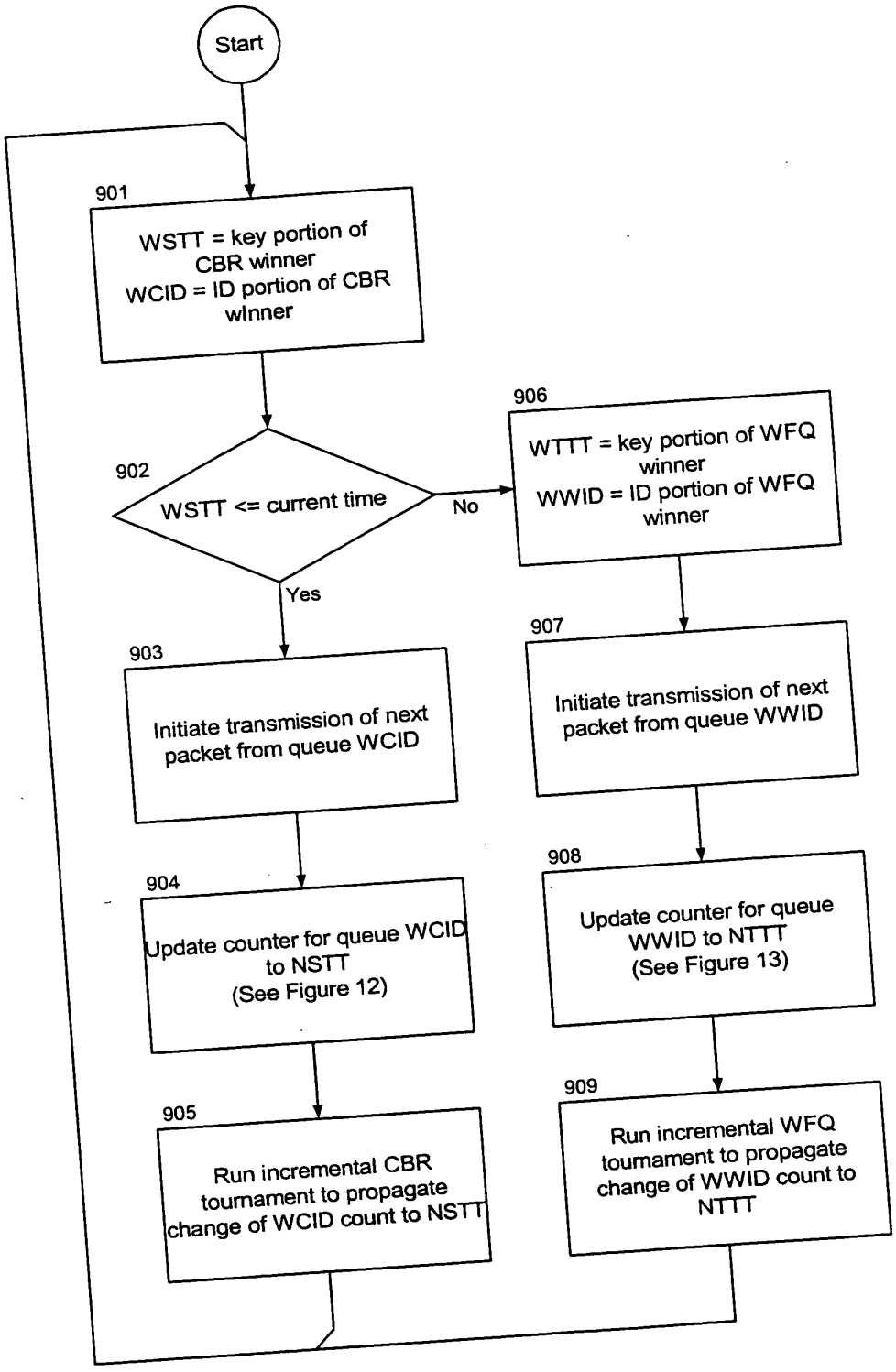
Start
901
WSTT = key portion of CBR winner
WCID = ID portion of CBR winner
902
WSTT <= current time
No
Yes
906
WTTT = key portion of WFQ winner
WWID = ID portion of WFQ winner
903
Initiate transmission of next packet from queue WCID
907
Initiate transmission of next packet from queue WWID
904
Update counter for queue WCID to NSTT
(See Figure 12)
908
Update counter for queue WWID to NTTT
(See Figure 13)
905
Run incremental CBR tournament to propagate change of WCID count to NSTT
909
Run incremental WFQ tournament to propagate change of WWID count to NTTT

Figure 14

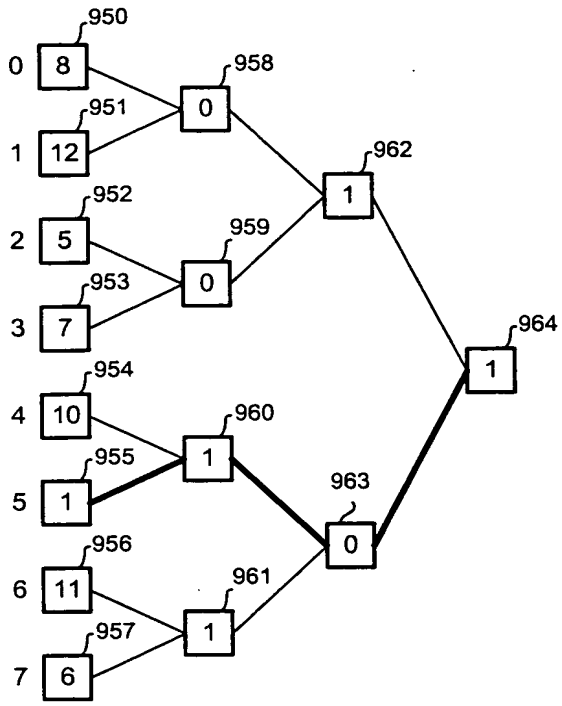

Figure 15

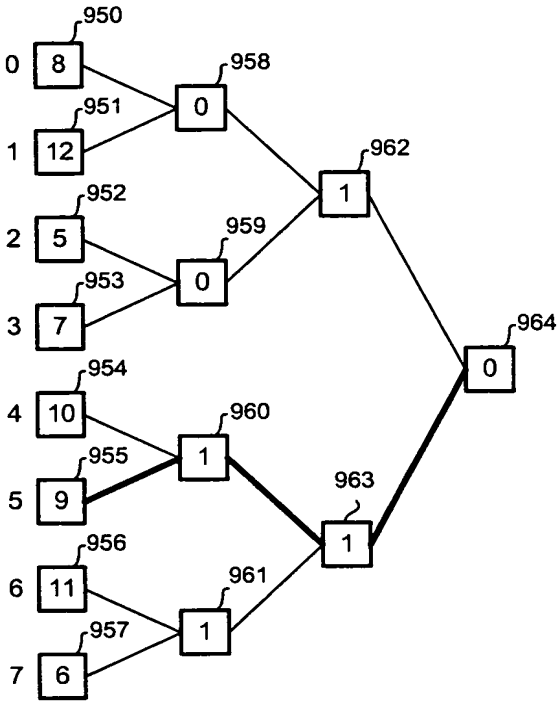

Figure 16

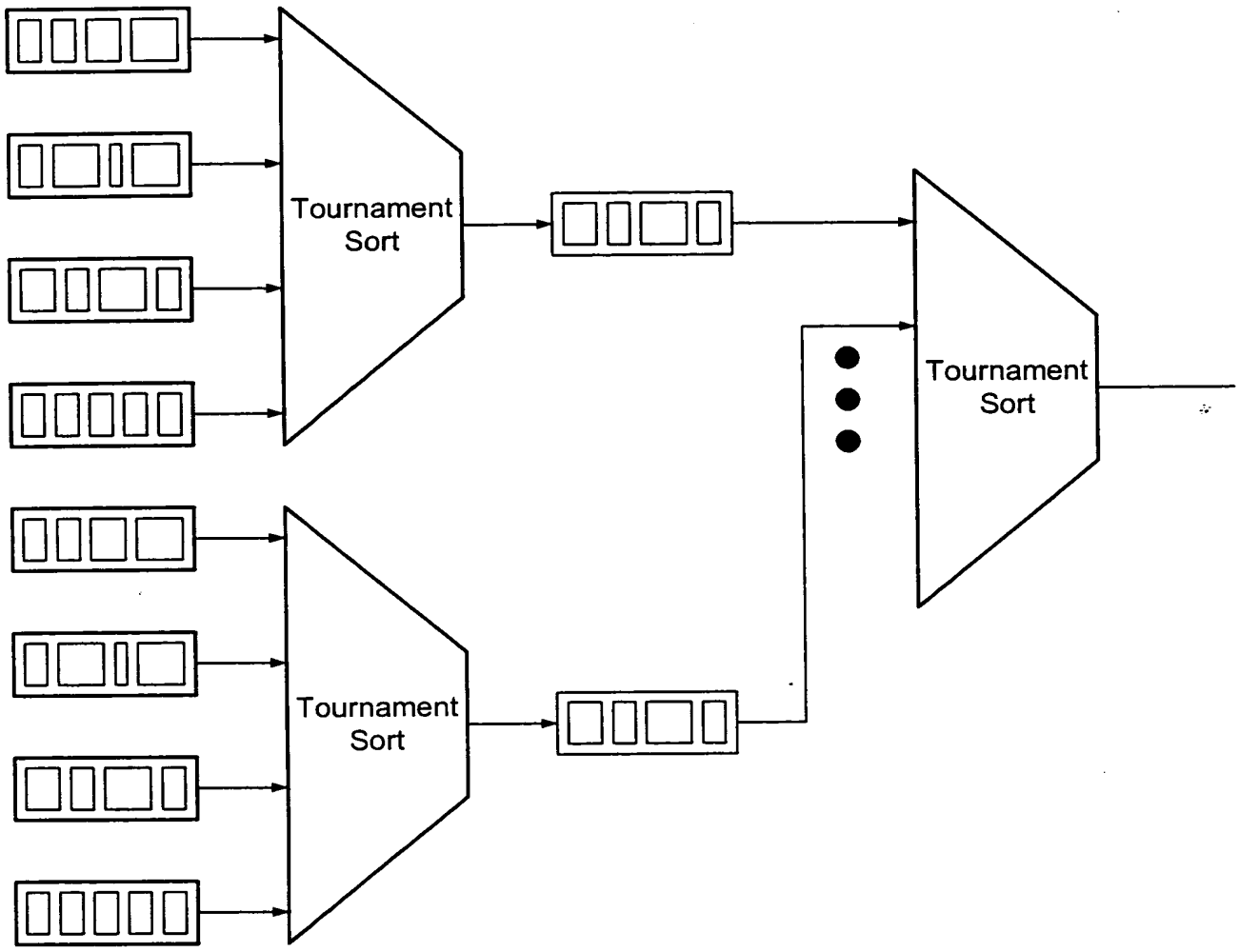

Figure 17

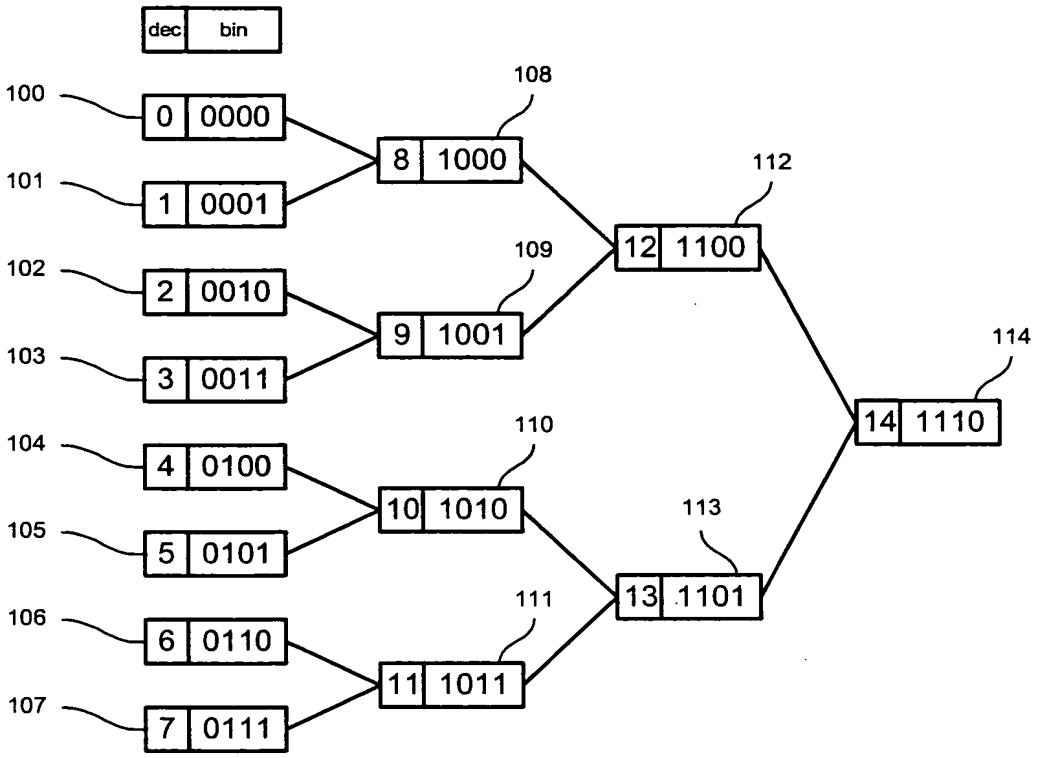
dec
bin
100
0
0000
101
1
0001
102
2
0010
103
3
0011
104
4
0100
105
5
0101
106
6
0110
107
7
0111
108
8
1000
109
9
1001
110
10
1010
111
11
1011
112
12
1100
113
13
1101
114
14
1110

Figure 18

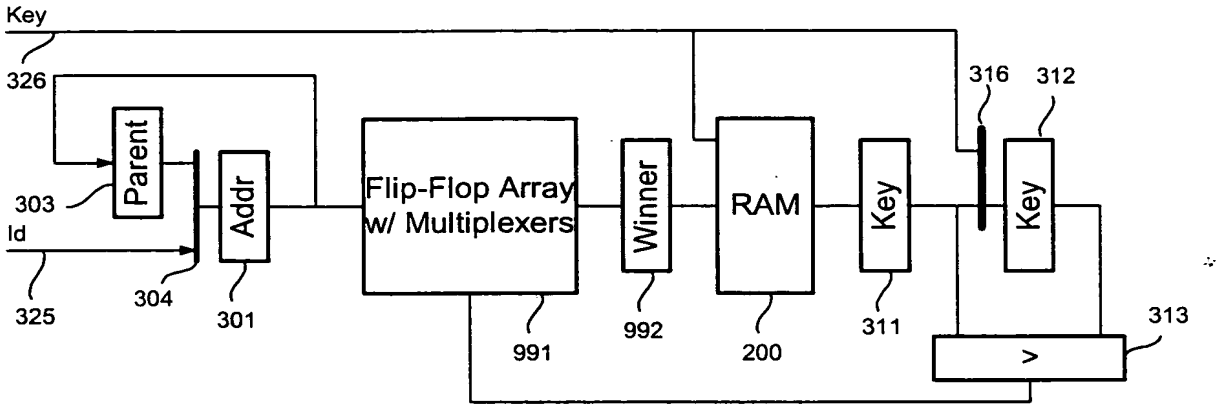
Key
326
316
312
Parent
303
Addr
Flip-Flop Array
w/ Multiplexers
Winner
RAM
Key
Key
Id
325
304
301
991
992
200
311
313
>

Figure 19

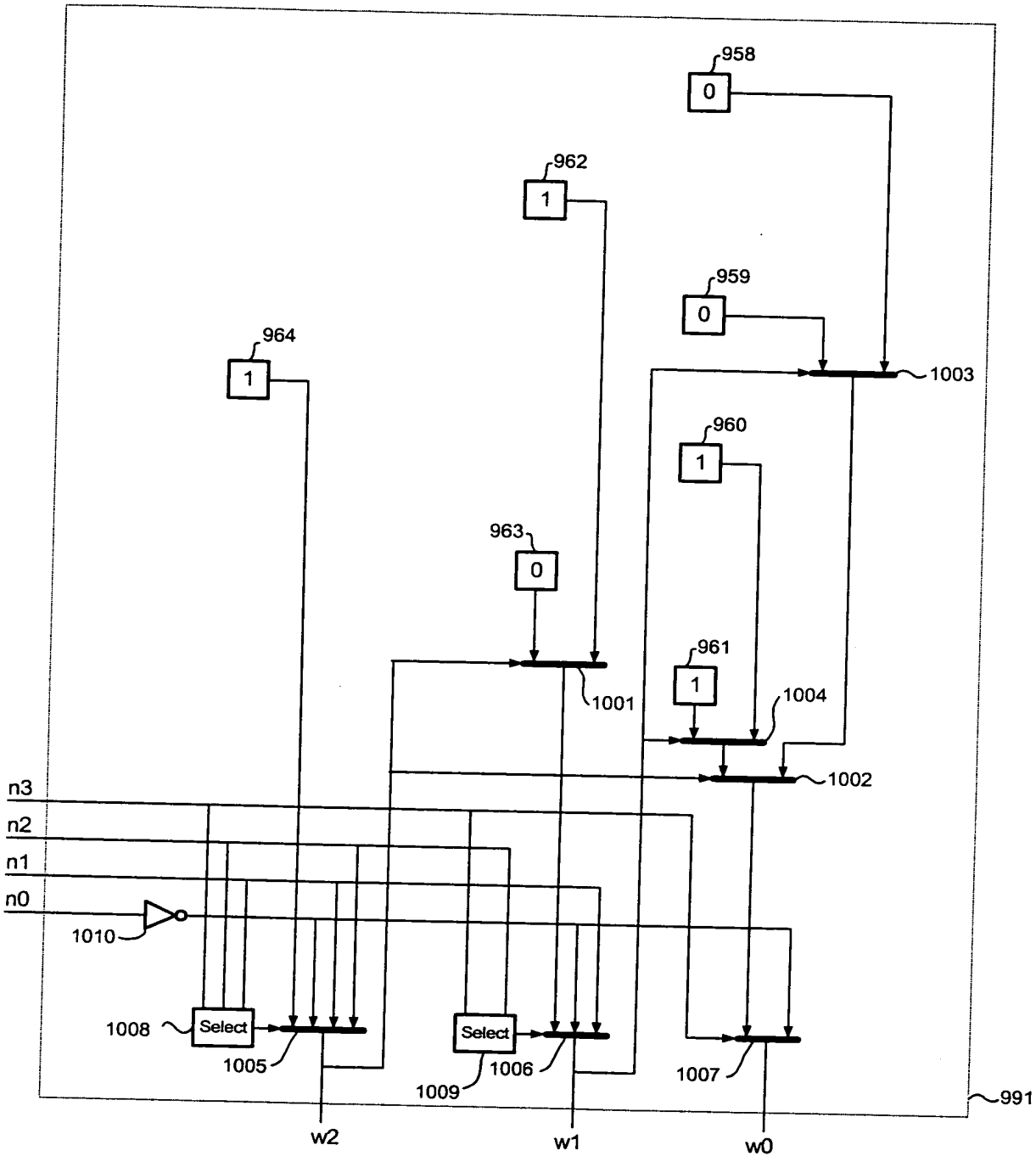
958
0
962
1
959
0
964
1
1003
960
1
963
0
961
1
1004
1001
1002
n3
n2
n1
n0
1010
1008
Select
1005
Select
1009
1006
1007
991
w2
w1
w0

Figure 20